

REMARKS

The present application was filed on July 21, 2003 with claims 1-18. In the outstanding Office Action dated March 25, 2004, the Examiner has: (i) objected to the drawings under 37 C.F.R. 1.83(a); (ii) rejected claims 1-18 under 35 U.S.C. §112, second paragraph as being indefinite; and (iii) rejected claims 1-18 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,707,102 to Morikawa et al. (hereinafter "Morikawa").

In this response, claims 1 and 14 have been amended. Applicants traverse the §112 and §103(a) rejections for at least the reasons set forth below. Applicants respectfully request reconsideration of the present application in view of the above amendments and the following remarks.

The Examiner has objected to the drawings for failing to show every feature of the invention specified in the claims (Office Action; page 2, first paragraph). Applicants respectfully traverse the objections to the drawings. Specifically, the Examiner contends that "the claimed shielding layer and its physical relationship with other device elements must be shown or the feature(s) canceled from the claim(s)" (Office Action; page 2, first paragraph). Applicants submit, however, that there is no "shielding layer" recited in any of the subject claims, but rather a "shielding structure" is recited in the claims. The shielding structure (e.g., shielding electrode) and its physical relation to other device elements is clearly illustrated in one or more of the figures. For example, with reference to FIG. 2 of the present application, an illustrative implementation of the shielding structure is shown as dummy gate 222. The term "dummy gate" as used throughout in the present specification is one example of the claimed shielding structure (see, e.g., Specification; page 6, line 25).

With regard to the objection to the drawings for failing to show a vertical diffused MOS device as recited in claim 9, Applicants submit that such feature is not essential for a proper understanding of the invention, but rather a vertical diffused MOS device is merely a specific type of MOS device, as is generically set forth in claim 1. Consequently, Applicants do not believe that such additional limitations of claim 9 need to be depicted in the drawings.

For at least the above reasons, Applicants assert that all elements recited in the claims that are necessary for a proper understanding of the invention are clearly depicted in the drawings.

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Accordingly, withdrawal of the objections to the drawings is respectfully solicited. In addition, Applicants hereby request an acknowledgment of the formal drawings filed on September 29, 2003 in the present application.

Claims 1-18 stand rejected under §112, second paragraph as indefinite “for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention” (Office Action; page 2, paragraph 5). The Examiner contends that the first source/drain region and second source/drain region recited in the claims “is not specifically addressed to imply a single or two transistors” (Office Action; page 2, paragraph 6). Applicants respectfully disagree with this contention. With regard to independent claims 1 and 14, it is clear from the respective preambles that these claims are directed to a single MOS device. Furthermore, it is clear from the specification that the terms first and second source/drain regions refer to either a source region or a drain region of the single MOS device. The specification states that:

because the MOS device is symmetrical in nature, and thus bidirectional, the assignment of source and drain designations in the MOS device is essentially arbitrary. Therefore, the source and drain regions may be referred to generally as first and second source/drain regions, respectively, where “source/drain” in this context denotes a source region or a drain region. (Specification; page 6, lines 8-12; emphasis added)

Changing the first source/drain region to read source region and changing the second source/drain region to read drain region in the subject claims, as suggested by the Examiner, is unnecessarily limiting since the source and drain regions of a given MOS device can be arbitrarily assigned.

For at least the above reasons, Applicants submit that claims 1-18 are not indefinite. Accordingly, withdrawal of the §112 rejection of claims 1-18 is respectfully solicited.

Claims 1-18 stand rejected under §103(a) as being unpatentable over Morikawa. With regard to independent claims 1 and 14, which are of similar scope, the Examiner contends that Morikawa discloses all of the elements set forth in the subject claims. While Applicants disagree with this contention, claims 1 and 14 have been amended to further clarify the invention. Specifically, claims 1 and 14, as amended, further define the shielding structure as being electrically connected to the first source/drain region “by way of a connection formed in an active area of the device between the

gate and the second source/drain region.” Support for this amendment can be found in the specification at, for example, page 12, lines 16-21, and in figure 2. Applicants submit that the prior art of record fails to teach or suggest at least this feature of the claimed invention.

Morikawa, with reference to FIGS. 1 and 2, discloses a shield conductive film 10 formed above an n-type semiconductor region 8, between a gate electrode 3 and a drain 9 of a MOSFET device. However, in contrast to the claimed invention, Morikawa discloses that the shield conductive film 10 is connected to a source 5 by way of wiring 13 which is connected to the shield conductive film 10 via a contact formed outside an active area of the device. Morikawa states, with reference to FIG. 1, that “wiring 13 is also electrically connected to the shield conductive film 10 via a contact hole 18, which is formed in the silicon oxide film 12 provided over the field oxide film 2 surrounding an active region L” (Morikawa; column 6, lines 10-14; FIG. 1; emphasis added). In the claimed invention, unlike the connection arrangement taught by Morikawa, the connection itself between the shield structure and the first source/drain region provides additional beneficial gate shielding so as to improve an effectiveness of the shielding structure.

For at least the reasons given above, Applicants submit that claims 1 and 14, as amended, are patentable over the prior art of record. Accordingly, favorable reconsideration and allowance of claims 1 and 14 are respectfully requested.

With regard to claims 2-13, which depend from claim 1, and claims 15-18, which depend from claim 14, Applicants submit that these claims are also patentable at least by virtue of their dependency from their respective base claims. Moreover, one or more of these claims define additional patentable subject matter in their own right. For example, claim 10, and claim 17 which is of similar scope, further define the shielding structure as being “formed relative to the gate such that a capacitance between the gate and the second source/drain region is minimized without substantially increasing a capacitance between the gate and the first source/drain region.” The prior art of record fails to teach or suggest at least this additional feature. Furthermore, the Examiner fails to indicate with any specificity where in Morikawa such features of claim 10 are disclosed.

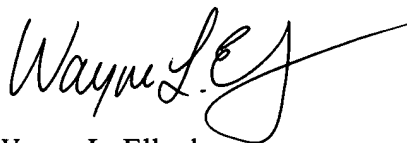
For at least the reasons set forth above, Applicants submit that claims 2-13 and 15-18 are patentable over the prior art of record, not merely by virtue of their dependency from respective

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claims 1 and 14, but also in their own right. Accordingly, favorable reconsideration and allowance of claims 2-13 and 15-18 are respectfully solicited.

In view of the foregoing, Applicants believe that claims 1-18, which are currently pending in the application, are in condition for allowance, and respectfully request withdrawal of the §112 and §103 rejections.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Wayne L. Ellenbogen", with a long horizontal flourish extending to the right.

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